

Achieving Zero Common Mode Voltage and Improved Linearity Relationship by a Novel Modulation Method

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Abstract—This paper proposed a new modulation strategy to eliminate common mode voltages in multilevel inverters. In this scheme which is explained for a 5-level modular inverter, all voltage vectors with zero common mode voltages can be classified into four categories and each two adjacent categories composed a segment. Synthesized voltage vectors that are an approximation to the reference vector belong to the segment in which the reference vector lies. Dwell times of these voltage vectors, depend on the distance between reference vector and the voltage vectors. This scheme leads to a good linearity relationship and low total harmonic distortion.

Index Terms— Common mode voltage, Multilevel modular inverter, Modulation, Linearity, THD

1 INTRODUCTION

The main purpose of the control for multilevel inverters is to synthesize the output voltages corresponding to the desired sinusoidal waveforms. Many modulation schemes have been developed with considerations to harmonic generation, linearity relationship or common mode voltage eliminations [1-3]. Due to the resulting overall inverter performance, simplicity both in hardware and software, space vector modulation is still considered as a suitable choice for multilevel PWM inverters [4].

One of the simplest ideas to control the output voltages based on SVM is to select adjacent voltage vectors. The dwell times of these vectors is based on time-averaging principle which may lead to complicated calculations. In some schemes to achieve simpler calculations, only nearest vector to the reference vector will be delivered [1, 5]. Figure 1(a) shows a modular five-level PWM inverter. Each leg consists of four bidirectional chopper-cells which have been shown in figure 1(b).

These cells which are the basic components of the MMC topology known as a sub-module. Each sub-module consists of a dc capacitor and two IGBTs which composed a bidirectional chopper. Its output voltage is

either equal to the capacitor voltage V_c or zero. Also it should be noted that to avoid short-circuiting, operation of the switches has a complementary role in a sub-module. So when either of the sub-modules is turned-on, the other one of the same sub-module must be switched off. Since the number of chopper-cells per leg is four, five-level (9-level in line-to-line) PWM waveforms will be produced.

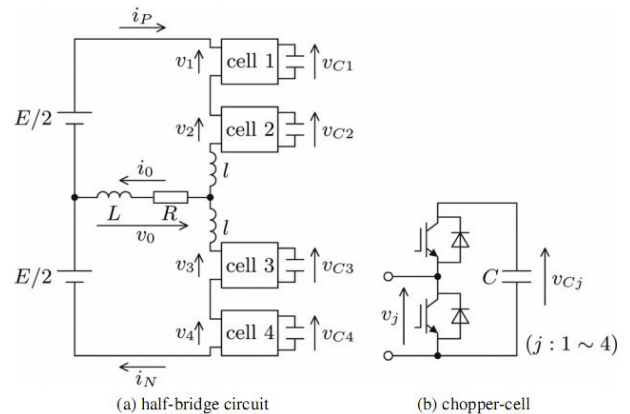


Figure 1. circuit configuration of a modular multilevel converter

2 PROPOSED MODULATION ALGORITHM

One of the easiest space vector modulation methods is to deliver the nearest voltage vector with respect to the reference vector [1]. Figure 2 represents the phase voltages, line to line voltage, and common mode voltage in a five-level inverter controlled by this scheme (using

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nearest vectors), operating with a modulation index of $m=0.9$ and fundamental frequency of 50Hz. Considering figure 2 (b) this modulation method generates an important amount of common mode voltages. Common mode voltages commutations can generate circulating currents that is the cause of bearing failures [6]. Therefore, to avoid these failures, this scheme is not recommended.

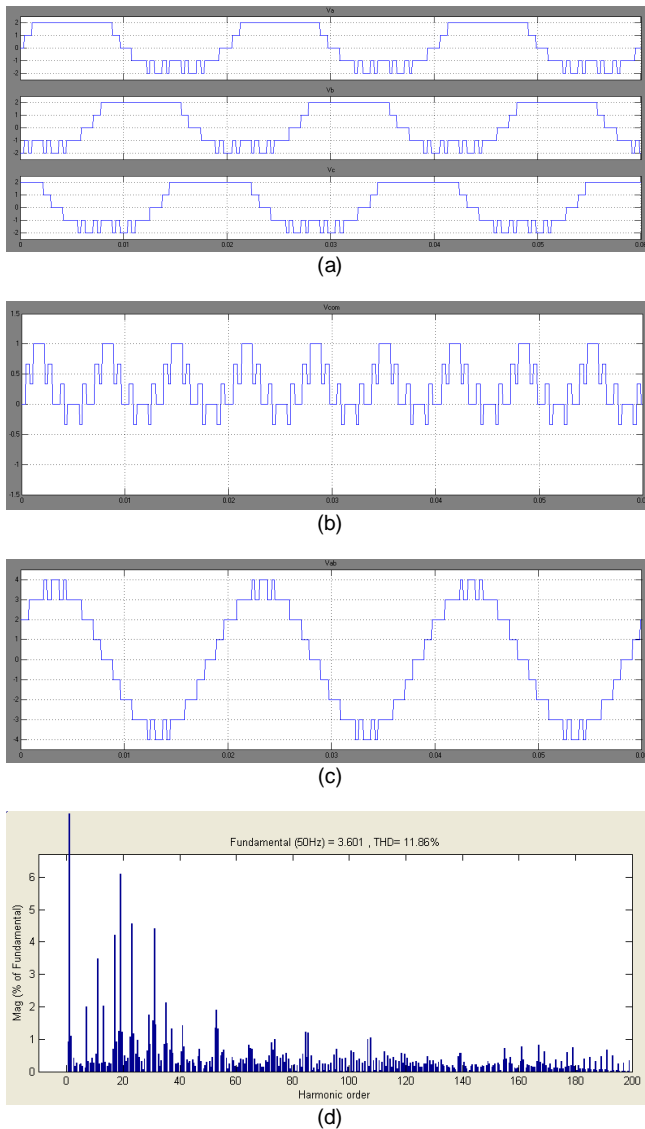


Figure 2. (a) Phase voltages, (b) common mode voltage, (c) line to line voltage, and (d) spectrum of line to line voltage in a five level inverter using nearest vectors method with $m=0.9$

To modify this scheme, only voltage vectors which have zero common mode voltages can be used. This restriction of vectors increases the distance between reference vector and the vectors of space vector diagram. So the error of the generated voltage with respect to the reference will be

increased. Consequently as shown in figure 3, the linear relationship between fundamental voltage and modulation index will be decreased [1]. The proposed method in this paper, will completely eliminate common mode voltages, and will improve the linear relationship.

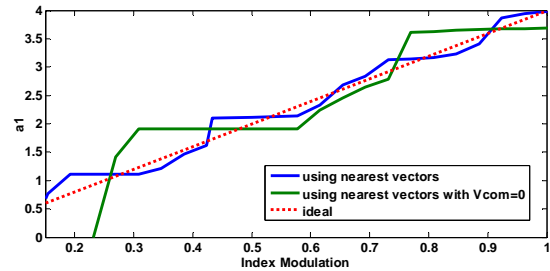


Figure 3. Comparison of fundamental voltage (a_1) versus index modulation (m) in a 5-level inverter ($1pu=V_{cc}$)

In the proposed method, voltage vectors with zero common mode voltages are classified into four categories and each category is located on a hexagonal in space vector diagram as shown in figure 4. It should be noted that the zero voltage vector (2, 2, 2) by itself is a category.

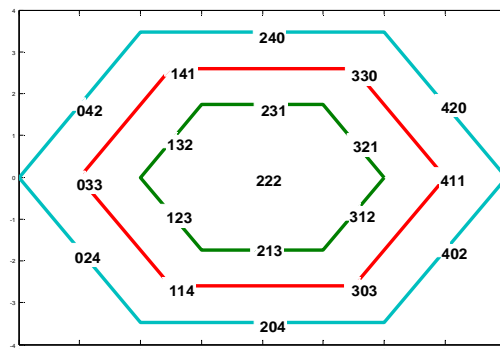


Figure 4. Representation of voltage vectors with zero common mode in a five-level inverter.

Each of categories creates a circle. Therefore as shown in figure 5, circles with radiuses R_1 and R_3 have been embedded in green and blue hexagonals respectively. Second hexagonal that is red colored, has been embedded in the circle with radius R_2 .

It should be noted that the first category which is a zero vector, is a circle with zero radius, (i.e. a simple dot). Each two adjacent circles compose a segment as shown in Table 1. Thus d-q plane is divided into 3 segments.

Considering table 1, each of centric circles with R_1 and R_2 radiuses has been used in two segments. Therefore to

specify the border of each segment it should be determined that reference vector is closer to which of adjacent circles.

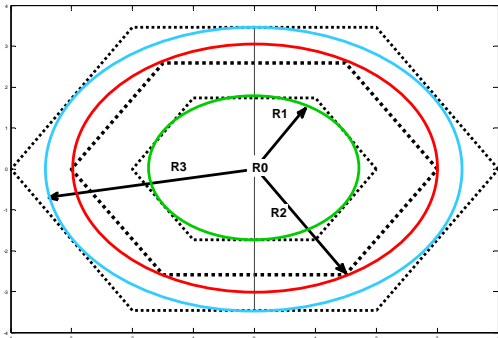


Figure 5. Representation of circles with radii R0, R1, R2 and R3

TABLE 1
 TWO ADJACENT CIRCLES IN EACH SEGMENT

Numer of segments	Used circles
1	Circle 0 & circle 1
2	Circle 1 & circle 2
3	Circle 2 & circle 3

For example to determine the border of segment 1:

$$\left| |V_{ref}| - R_0 \right| < \left| |V_{ref}| - R_2 \right| \Rightarrow |V_{ref}| < \frac{R_0 + R_2}{2} \quad (1)$$

So :

$$\begin{aligned} \text{if } |V_{ref}| < \frac{R_0 + R_2}{2} &\Rightarrow \text{segment 1} \\ \text{if } \frac{R_0 + R_2}{2} < |V_{ref}| < \frac{R_1 + R_3}{2} &\Rightarrow \text{segment 2} \\ \text{if } \frac{R_1 + R_3}{2} < |V_{ref}| &\Rightarrow \text{segment 3} \end{aligned} \quad (2)$$

When the reference vector falls in one of the segments the voltage vectors in that segment are selected to synthesize

the desired voltage vector. the dwell times of these vectors depend on distance between reference vector and them. To determine the dwell times, parameter m is defined as:

$$m = \frac{|V_{ref}|}{R_i} \times \frac{60^\circ}{2} \quad (3)$$

The main idea of this scheme is based on specifying $2m^\circ$ of each sector as shown in figure 6, to the voltage vectors which are located on circle with radius R_i . The residue of sector is specified to the vectors of other circle which is composed the segment. So if the reference vector will be closer to circle with radius R_i , the section of sector which is dedicated to this circle will be greater.

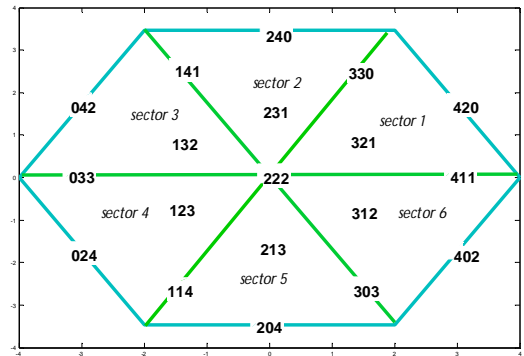


Figure 6. Representation of sectors and voltage vectors in each sector.

3 SIMULATION RESULTS

the waveform of figure 7 has been measured with $m=.9$ and an output frequency of 50Hz. Switching frequency is 5kHz.

Figure 8 represents a comparison of THD diagram between previous and proposed methods while both of them eliminate common mode voltages. Considering figure 8, THD diagram in mentioned schemes is similar especially at higher modulation indexes.

Figure 9 shows the comparison of linearity relationship between two mentioned methods. One of the disadvantage of previous method is to have zero fundamental voltage up to $m=.25$ which is removed by

the proposed method. Considering this figure it can be concluded that the linearity of proposed method is better than the previous method.

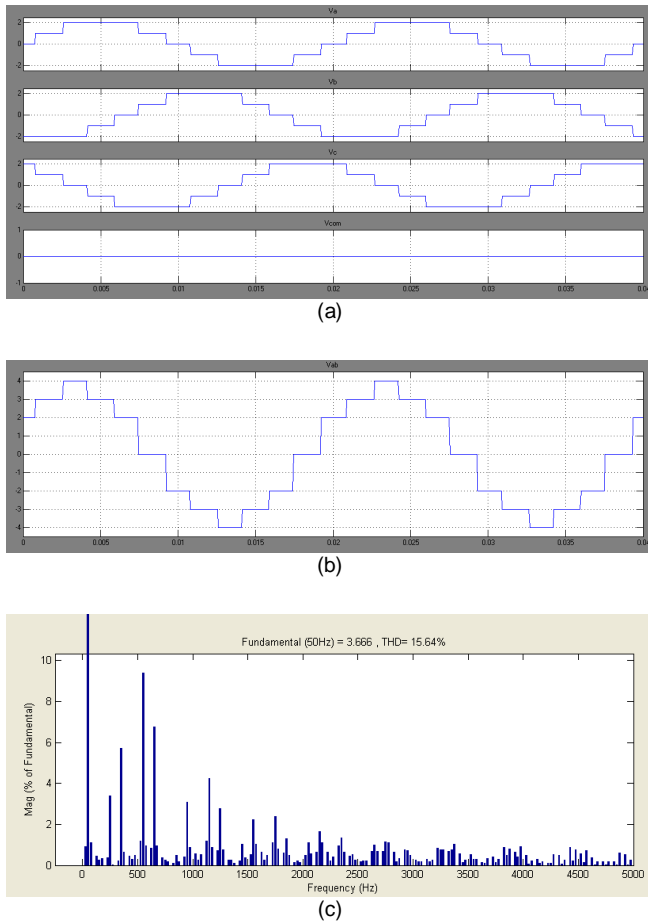


Figure 7. (a) Phase and common mode voltages, (b) line to line voltage, and (d) spectrum of line to line voltage in a five level inverter using proposed method with $m=0.9$

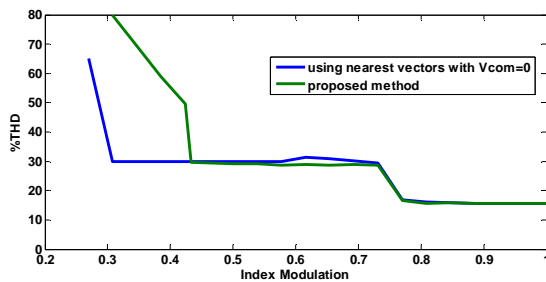


Figure 8. Comparison of total harmonic distortion (THD) versus modulation index (m) in a five-level.

To improve the linearity relationship in the proposed method, the margin of the first segment can be decreased. Applying this change will lead to a smaller jump in lower

modulation indexes. Also because of the steep slope in the second segment, its margin can be decreased. Finally as shown in figures 10 and 11, the relationship will be more linear while THD diagram will have small variations compared to the former proposed method.

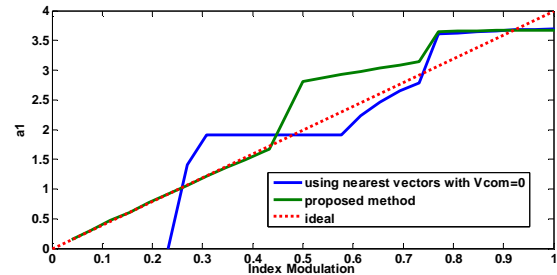


Figure 9. Comparison of fundamental voltage (a_1) versus modulation index (m) in a five-level inverter ($1pu=V_{cc}$).

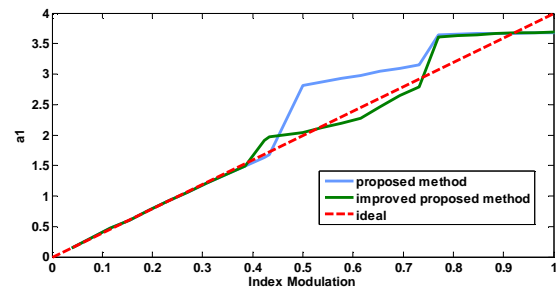


Figure 10. Comparison of fundamental voltage (a_1) versus modulation index (m) in a five-level inverter ($1pu=V_{cc}$)

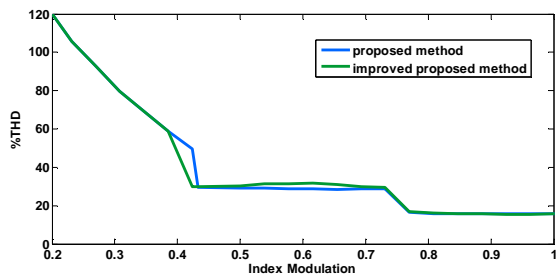


Figure 11. Comparison of total harmonic distortion (THD) versus modulation index (m) in a five-level inverter

4 CONCLUSION

This paper proposed a new SVM scheme to eliminate common mode voltages in multilevel inverters. In this scheme, the space vectors are restricted to vectors with zero common mode voltages and are classified into four

categories. Except the first category which has a zero voltage vector, the next ones have six voltage vectors located on three hexagonals. Each two adjacent categories composed a segment that their vectors are used to synthesize the reference vector. So each segment has two categories of vectors, and the dwell times of them are depend on the distance between reference vector and these vectors. This scheme has a good linearity relationship and low total harmonic distortion.

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